MERRICK1 User Manual

Issue – 1.0

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Kit Contents

You should receive the following items with your Merrick1 Board:

1 - Merrick1 Board
2 - Prog2 (parallel port) or Prog3 (USB) programming cable

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Foreword

PLEASE READ THIS ENTIRE MANUAL BEFORE PLUGGING IN OR POWERING UP YOUR MERRICK1 BOARD.
PLEASE TAKE SPECIAL NOTE OF THE WARNINGS WITHIN THIS MANUAL.

Trademarks

Spartan-6, ISE, EDK, Webpack, Xilinx are the registered trademarks of Xilinx Inc, San Jose, California, US.

Merrick1 is a trademark of Enterpoint Ltd.

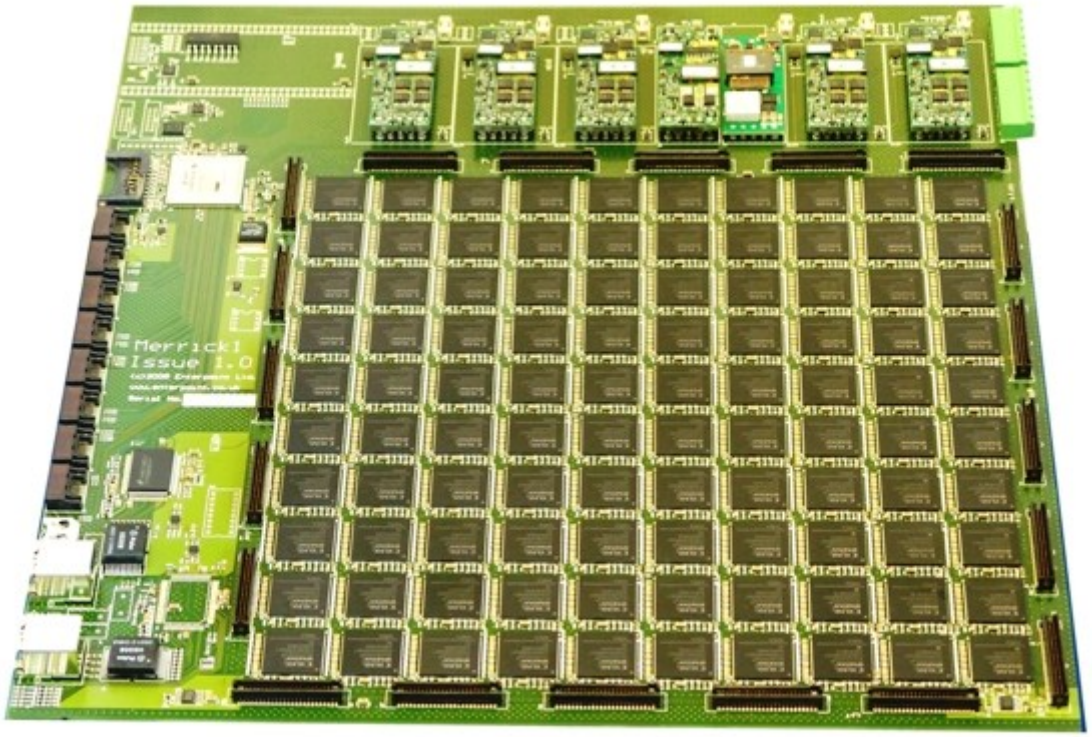


Figure 1 – Merrick1 Board

Introduction

Welcome to your Merrick1 board. Merrick1 is Enterpoint's first High Performance Computing product aimed at custom high performance processing tasks such as:

Cryptography
Artificial intelligence e.g. Neural Networks and Genetic Algorithms
ASIC prototyping and Emulation
Biometric Modelling and Analysis
Data Mining, Analysis and Extraction.
Financial Modelling and Analysis
Image Processing
Weather System Modelling and Analysis

and many other applications where a high degree of parallel processing is required.

The aim of this manual is to assist in using the main features of Merrick1.
There are features that are beyond the scope of the manual. Should you need to use these features then please email support@enterpoint.co.uk for detailed instructions.

In addition Merrick1 is supported by a wide range of add-on modules. Some examples of these include:

ADC 7927 MODULE
LED DOT MATRIX MODULE
BUTTONS/SWITCHES/SATA/MEMORY MODULE
RS232 AND RS485 HEADER MODULES
DP83816 ETHERNET MODULE
SD CARD MODULE
DDR2 MODULE
IDE/5V TOLERANT CPLD MODULE
USB MODULE
D/A CONVERTER MODULE
ADV70202 MODULE

We can also offer custom DIL Header modules should you require a function not covered by our current range of modules. Typical turn around for this service is 6-8 weeks depending upon quantity ordered and availability of components.

Custom Solutions

The modular nature of the Merrick1 design allows us to derive customer specific variants by removing part of the array and replacing with custom electronics. It is possible to implement these changes and build a prototype in a timescale as low as 4 weeks although 8-12 is our typical quote for a board of this complexity. NRE charges do apply for this service. Contact us on boardsales@enterpoint.co.uk for more details.

Merrick1 comes in a single variant based on an XC3SD3400A-4CSG484C Spartan-3A-DSP FPGA. Should you need more powerful or industrial or automotive grade FPGAs fitted please contact Enterpoint sales for a quote. Commercial -5 and industrial -4 grade devices are also available; another alternative offered is to fit XC3SD1800A devices allowing use of free WebpackTM ISE™ software with this board. Contact Enterpoint for details by emailing boardsales@enterpoint.co.uk or telephoning +44 (0) 121 288 3945.

Merrick1 Board

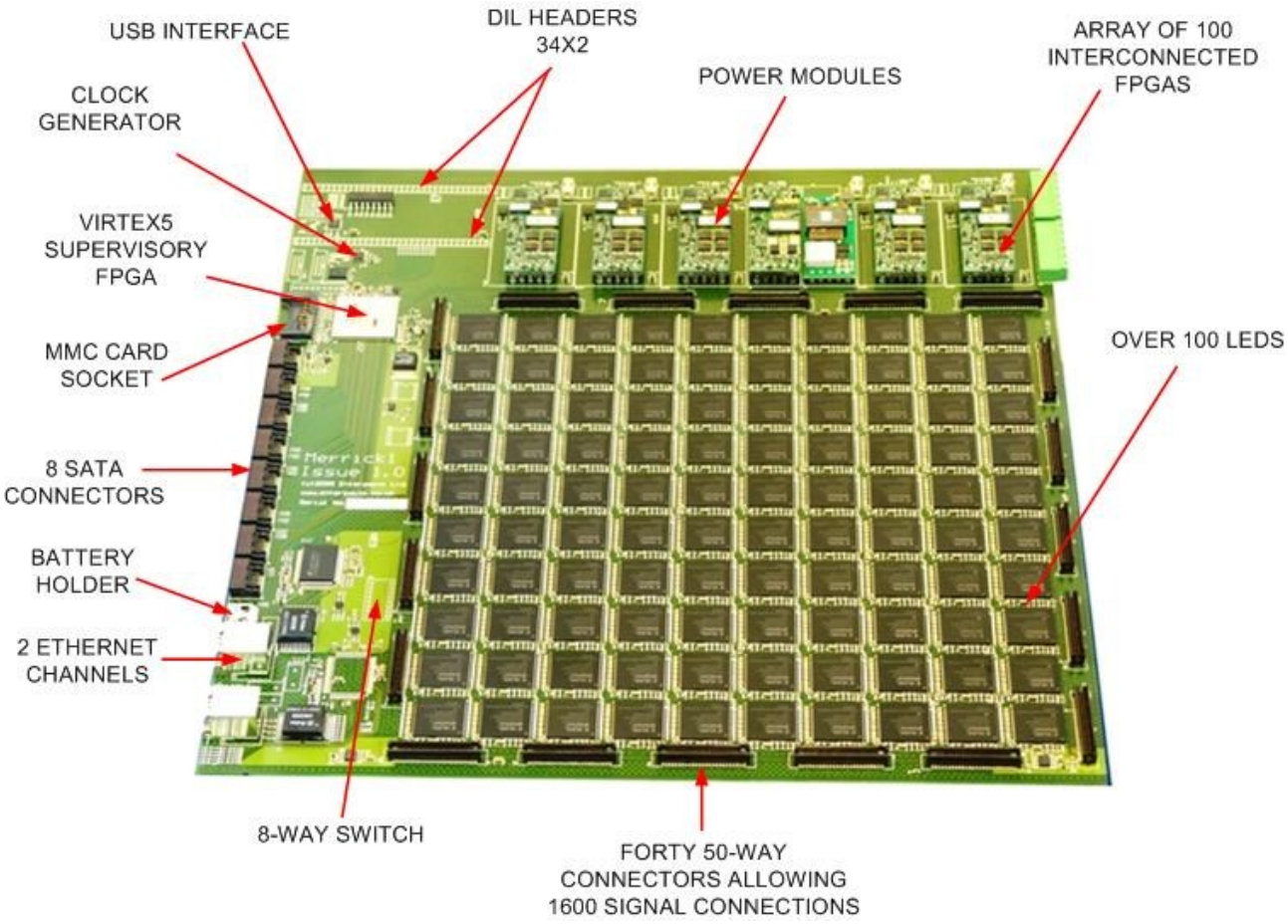


Figure 2 – Merrick1 Main Features

Power Input

Merrick1 is powered from a nominal 48V power supply via two 6pin connectors which have contacts rated at 12A maximum. These sockets are manufactured by Phoenix part no. 1757284 and accept Phoenix plug type 1792799 (available from Farnell and Digikey for example). Merrick1 will operate over an input voltage range of 36-72V, but the actual voltage chosen must be compatible with cooling fan power supply requirements.

Power Modules

There are five eighth brick 1.2V power modules on Merrick1. The main array of FPGAs is divided into 5 sections, each of 2 columns (=20 FPGAs), each of which has a dedicated 1.2V power module for the FPGA core voltage. These modules are each capable of delivering 30A and are each protected by a fuse and monitored by an STM6720 Voltage monitor, with the resulting POK signals being routed to the Controller FPGA. They can be controlled individually from the Controller FPGA if it is necessary to switch off part of the main array (e.g. to conserve power). When the Controller FPGA is unconfigured these modules are switched off, so the POWER_ON_N_M signal for each block must be driven low to switch on each module. There is an LED near each module to indicate the presence of 1.2V. The connections between the Controller FPGA and the power modules are shown below.

SIGNAL	POWER MODULE	FPGA PIN
POWER_ON_N_M1	U6_P1	Y21
POWER_ON_N_M2	U6_P2	AA20
POWER_ON_N_M3	U6_P3	AB10
POWER_ON_N_M4	U6_P4	AB11
POWER_ON_N_M5	U6_P5	AB21
POK1	U6_P1	AB20
POK2	U6_P2	AC11
POK3	U6_P3	AB12
POK4	U6_P4	AB19
POK5	U6_P5	AA18

The Merrick board is designed to accept quarter brick modules as an alternative for applications where a greater Array FPGA core current is required. Currents of up to 100A per section could be accommodated.

There is one eighth brick 3.3V 30A power module on Merrick1 which supplies power to the peripherals and the DIL headers, and has an indicator LED and is monitored by the Controller FPGA on **Pin D25**. It will not power-up until the 2.5V module is ON.

There is one eighth brick 2.5V 30A module which powers the array FPGA IO, the Ethernet devices, the Controller FPGA VCCAUX and some Controller IO banks.

There is also a small 6A power module which supplies 1.2V to the Controller FPGA.

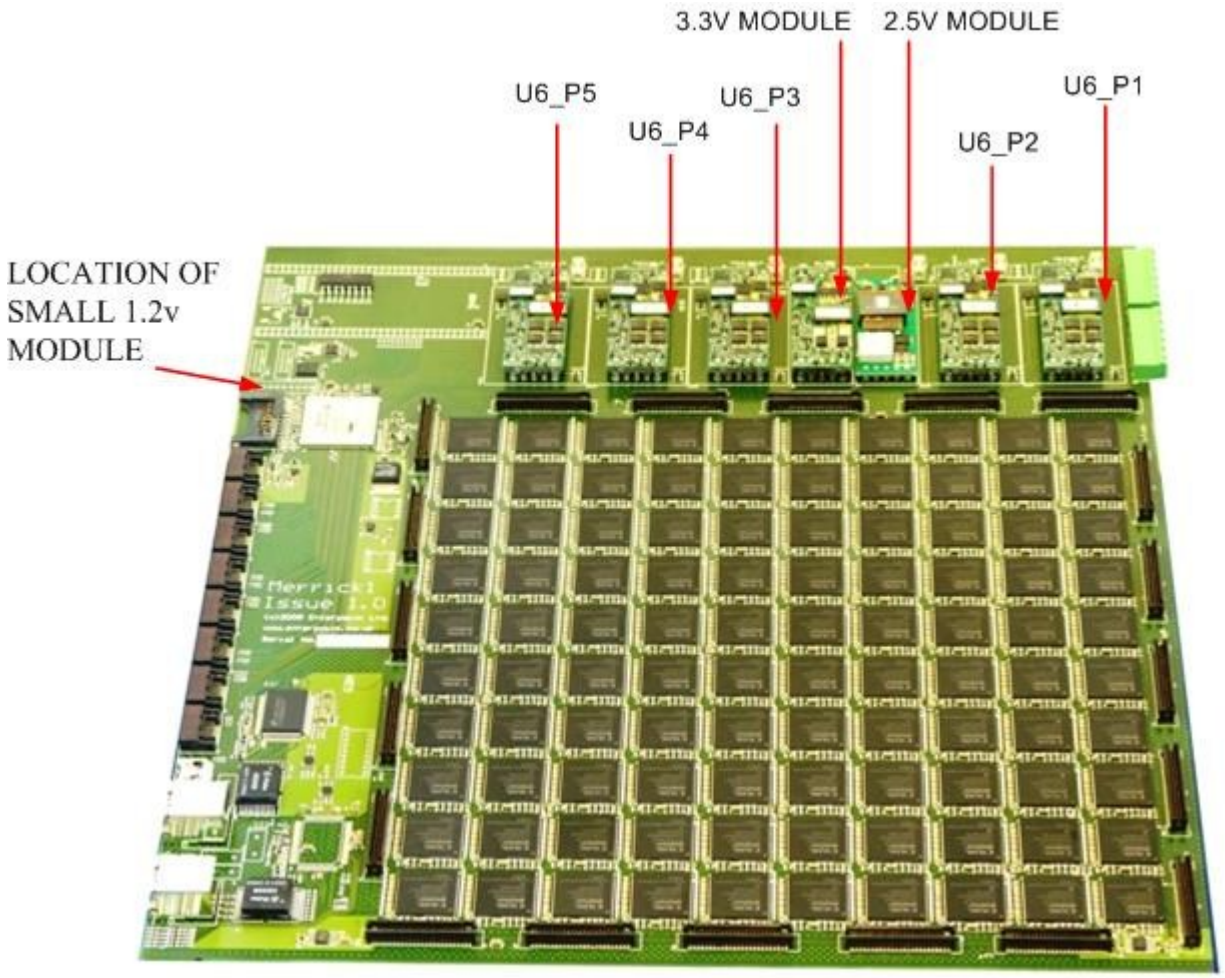


Figure 3 – Merrick1 Power Supply Modules

Power Regulators

In addition to the 7 power modules these are 6 power regulators on Merrick1. An AP7167 supplies 1V to the MGT IOs of the Controller FPGA, which service the Ethernet connections. ANLT1963 device generates a separate 1.2v supply , also for the Controller MGT interface. Two AP7167 devices each generate 1.8V, one for each Ethernet device. Two LP2995 regulators provide 1.25V reference voltages for the two Ethernet devices.

WARNING – THE POWER REGULATORS AND MODULES MAY BECOME HOT IN NORMAL OPERATION ALONG WITH THE BOARDS THERMAL RELIEF. PLEASE DO NOT TOUCH OR PLACE HIGHLY FLAMABLE MATERIALS NEAR THESE DEVICES WHILST THE MERRICK1 BOARD IS IN OPERATION.

Programming Merrick1

There are two JTAG connectors on Merrick1: J1, which is the JTAG programming interface for the Controller FPGA, and J61, which is used to program the Array FPGAs.

The JTAG connectors have a layout as follows:

LEFT EDGE OF BOARD

3V3	TMS	TCK	TDO	TDI	NC	NC
GND	GND	GND	GND	GND	GND	GND

Figure 4 – Merrick1 JTAG connectors

PROGRAMMING THE CONTROLLER FPGA

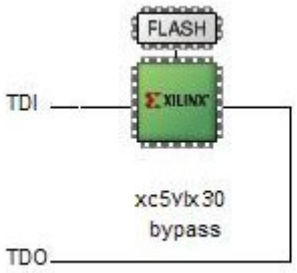
The JTAG chain displayed on the Xilinx programming software iMPACT will show a single device, the Virtex5 FPGA. Access to the SPI Flash memory (M25P128) will enable non-volatile programming of the Controller FPGA.

1. Programming the FPGA directly.

Direct JTAG programming of the Virtex5 FPGA is volatile and the FPGA will lose its configuration every time the board power is cycled. For sustained use of an FPGA design programming the design into the Flash memory is recommended (see 2 and 3 below).
Direct JTAG programming using .bit files is useful for fast, temporary programming during development of FPGA programs. Right click the icon representing the Virtex5 FPGA and choose 'Assign New Configuration File'. Navigate to your .bit file and choose 'OPEN'. The next dialogue box will offer to add a flash memory and you should decline. Right click the icon representing the Virtex5 FPGA and choose 'Program'. On the next dialogue box ensure that the 'Verify' box is not checked. (If it is you should uncheck it, failure to do this will result in error messages being displayed). Click OK. The Virtex5 will program. This process is very quick (typically a few seconds)

2. Programming the SPI flash memory using Boundary Scan.

Once the SPI Flash memory has been programmed, the Spartan-6 device will automatically load from the Flash memory at power up. Generation of suitable Flash memory files (.mcs) can be achieved using ISE iMPACT's Prom File Formatter.
Right click on the icon representing the Spartan-6 and choose 'Add SPI/BPI Flash' Navigate to your programming file (.mcs) and click OPEN. Use the next dialogue box to select SPI flash and M25P128. Data width should be set to 1. The flash memory should appear as shown below.



Right click on the icon representing the flash memory and choose ‘Program’ to load your program into the device. It is recommended that options to ‘Verify’ and ‘Erase before programming’ are chosen. Otherwise all defaults can be accepted. The programming operation will take some time (at least 3 or 4 minutes).

PROGRAMMING THE ARRAY FPGAS

The second JTAG connector (J61) is used to program the Array FPGAs. The Arrangement of FPGAs being programmed is controlled by the Controller FPGA configuration and the connections between J61 and the Controller FPGA are shown below:

J61 PIN	SIGNAL	FPGA PIN
4	SECONDARY_TMS	B16
6	SECONDARY_TCK	C17
8	SECONDARY_TDO	B17
10	SECONDARY_TDI	A17

The Array FPGAs are arranged in five blocks of 20 (2 adjacent columns of FPGAs per block) for programming and these can be individually turned on and off as required. Partial array operation is possible e.g. to conserve power and decrease programming time. Simple assignment operations in the configuration code are used to link the 5 array JTAG chains together. There are 10 TCK and TMS signals, one for each column of FPGAs, the TCK signals being terminated at the end of the column: The connections between the array JTAG signals and the Controller FPGA are shown below.

SIGNAL	SECTION5 COLUMNS 1-2		SECTION4 COLUMNS 3-4		SECTION3 COLUMNS 5-6		SECTION2 COLUMNS 7-8		SECTION1 COLUMNS 9-10	
LTDI	G11		H19		H18		G16		G15	
LTDO	Y16		AA14		AA13		Y7		AA17	
	COL 1	COL 2	COL 3	COL 4	COL 5	COL 6	COL 7	COL 8	COL 9	COL10
LTCK	AA9	AB9	AC9	AD9	AD8	AC8	AC7	AD6	AF3	AF4
LTMS	AD14	AD13	AE13	AF13	AF14	AF15	AE15	AD15	AD16	AE16

For example if the secondary JTAG chain was required to only address columns 1 and 2 of the Array FPGAs, the Controller FPGA would make the following assignments:

```
LTMS1 <= SECONDARY_TMS
LTMS2 <= SECONDARY_TMS
LTCK1 <= SECONDARY_TCK
LTCK2 <= SECONDARY_TCK
LTDI1  <= SECONDARY_TDI
SECONDARY_TDO <= LDTO1
```

For all columns to be programmed the following assignments would be made:

```
ALL 10 LTMS SIGNALS <= SECONDARY_TMS
ALL 10 LTCK SIGNALS <= SECONDARY_TCK
LTDI1 <= SECONDARY_TDI
LTDI2 <= LTDO1
LTDI3 <= LTDO2
LTDI4 <= LTDO3
LTDI5 <= LTDO4
SECONDARY_TDO <= LDTO5
```

Once the Controller FPGA has been configured to link the required Array FPGA JTAG connections to J61 the Array JTAG chain should be visible on an iMPACT boundary scan. Programming of the Array FPGAs is achieved using a .bit file and so is volatile.

The PROG_B signals for each column of Array FPGAs are connected together and the resulting 10 signals are routed to the Controller FPGA as shown below:

ARRAY COLUMN	FPGA PIN – PROG B
1	AE10
2	AD10
3	W8
4	W9
5	AD11
6	AE11
7	V9
8	V8
9	AE12
10	AF12

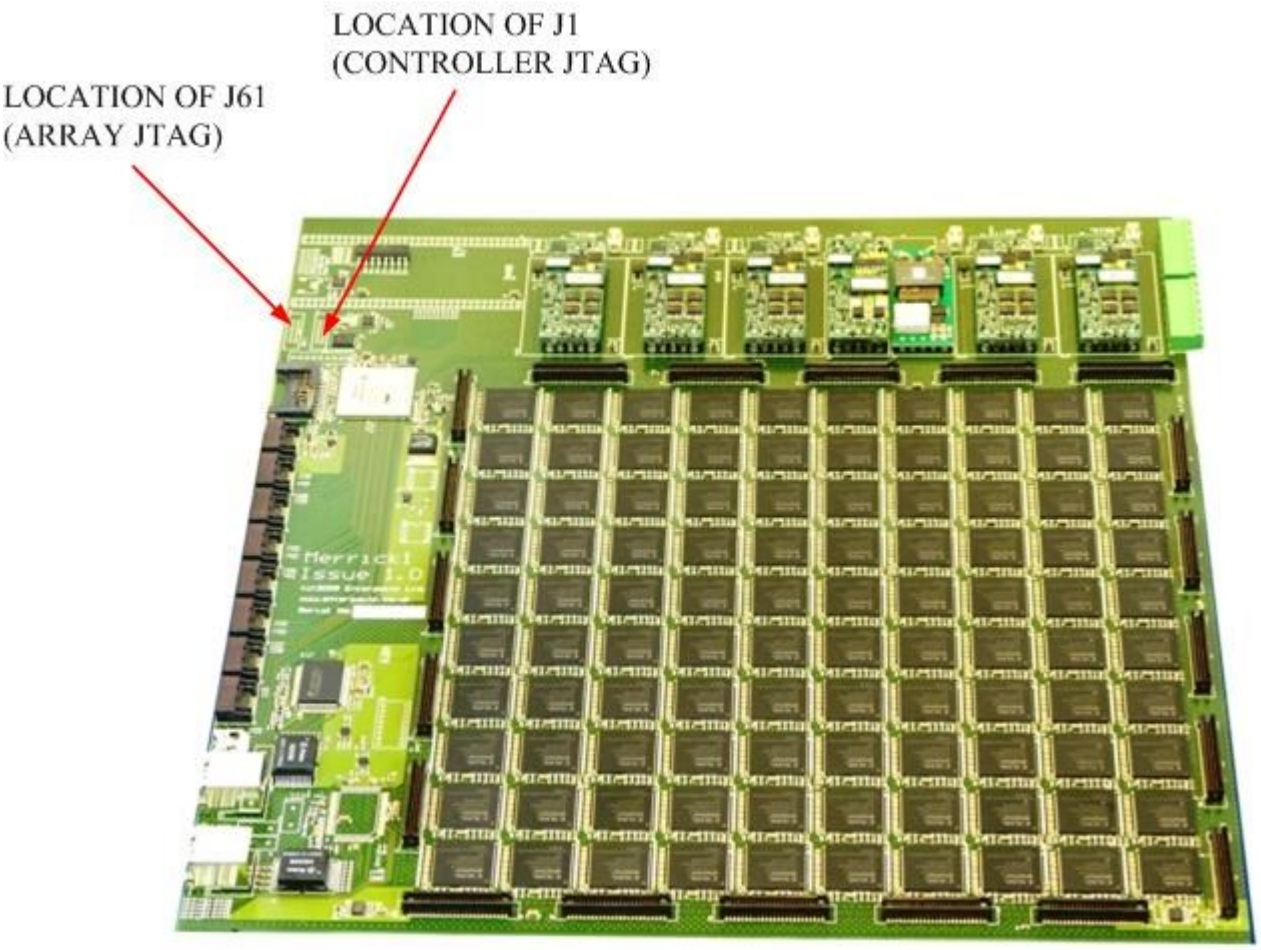


Figure5 – Merrick1 JTAG connectors

Controller FPGA

The Merrick1 controller FPGA is a Xilinx™ Virtex™-5 XC5VLX30T. Signals from the Ethernet, USB, MMC card, SATA and DIL expansion sockets are routed to this FPGA, Also 14 connections are routed from this FPGA to each column of Array FPGAs in a 'daisy chain' arrangement, so that there are a total of 140 routes between the controller and the array, with a maximum of 14 routes to any single array FPGA. Column routes via the Controller FPGA can be used for patching between FPGAs not adjacent in the array. The primary intention of these column routes is to distribute clock signals clocks but they may be used in any fashion desired. These wires are configured as 7 differential pairs but may be used single ended. Termination (nominally 50 ohms) to 1.25V is implemented on each wire at the end of each column. The Controller FPGA can also be configured to implement termination.

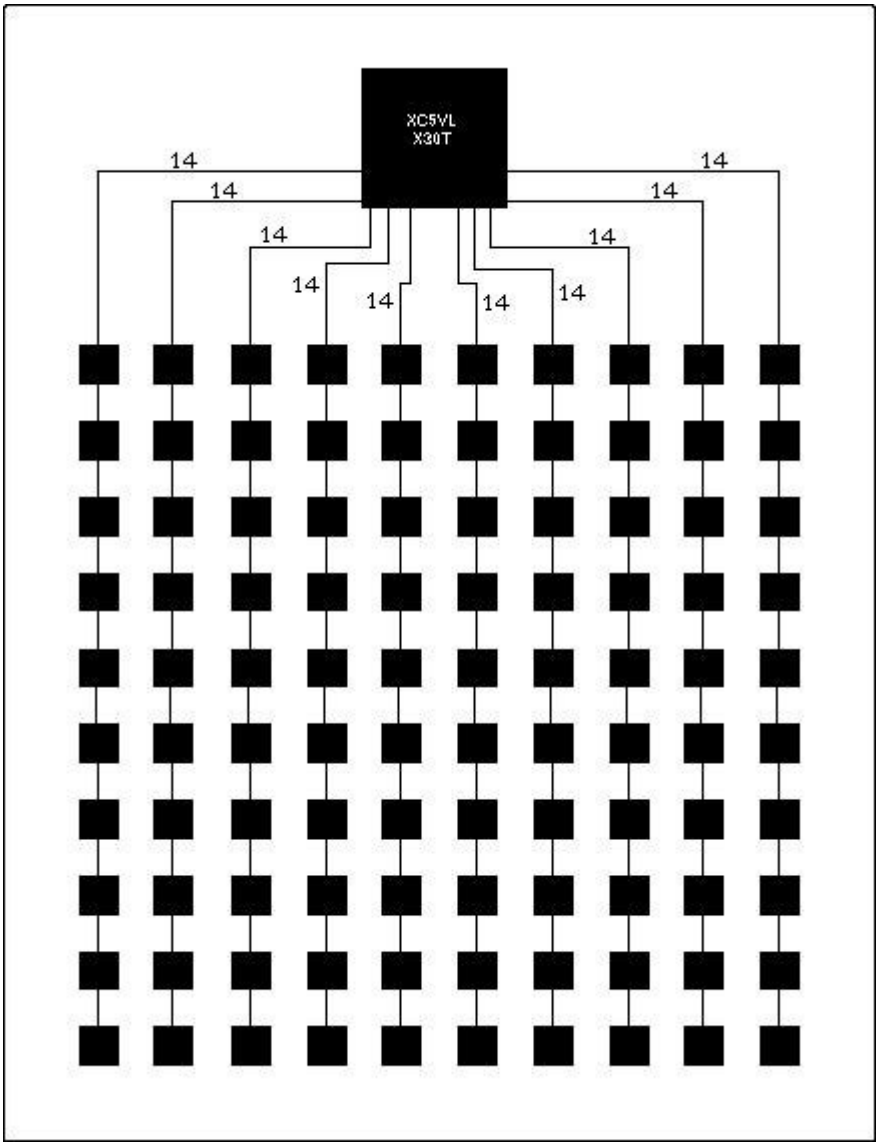


Figure6 – Interconnections between Controller and Array FPGAs

The connections between the Controller FPGA and the Array are shown below, with signal names using the convention CLOCKx_My, where x denotes the column number and y denotes the signal number

SIGNAL	SIGNAL NAME	CONTROLLER FPGA CONNECTIONS									
		Col.1	Col.2	Col.3	Col.4	Col.5	Col.6	Col.7	Col.8	Col.9	Col.10
1	CLOCKx_M0	H21	K21	M24	G26	V24	Y25	AA24	AD24	AB22	AF17
2	CLOCKx_M1	G20	J21	M25	F25	U24	Y26	AB25	AD25	AC22	AE17
3	CLOCKx_M2	G24	J26	L25	N23	U22	W25	V26	AE26	AC23	Y22
4	CLOCKx_M3	F24	J25	K26	N24	T22	W26	U26	AE25	AC24	A22
5	CLOCKx_M4	G25	K25	T23	R25	AD21	AE20	AF19	E16	G14	F17
6	CLOCKx_M5	H26	L24	T24	P25	AC21	AF20	AF18	D16	H13	G17
7	CLOCKx_M6	E25	J23	H9	T25	V23	AE23	V22	E15	G12	F19
8	CLOCKx_M7	E26	H23	G10	U25	W24	AF23	U21	D15	F13	E18
9	CLOCKx_M8	F22	L22	P23	F20	W21	AD23	R26	N21	E11	F14
10	CLOCKx_M9	F23	L23	P24	G21	V21	AE22	P26	M21	F12	F15
11	CLOCKx_M10	H22	K23	R22	M26	AA23	AD20	AD18	D18	D13	AF9
12	CLOCKx_M11	G22	K22	R23	N26	AB24	AD19	AE18	E17	D14	AF10
13	CLOCKx_M12	E22	J24	M22	E21	R21	W23	AB26	AD26	AF24	AE21
14	CLOCKx_M13	E23	H24	N22	E20	P21	Y23	AA25	AC26	AF25	AF22

The Controller FPGA also connects to the two Ethernet Controllers, the SATA connectors, the two clock generators, two oscillators, the USB interface, 8 LEDs, 2 temperature sensors, an 8-way switch, the system fans and a Data Card holder. It also controls the Main Array JTAG chains and controls and monitors the Main Array power modules.

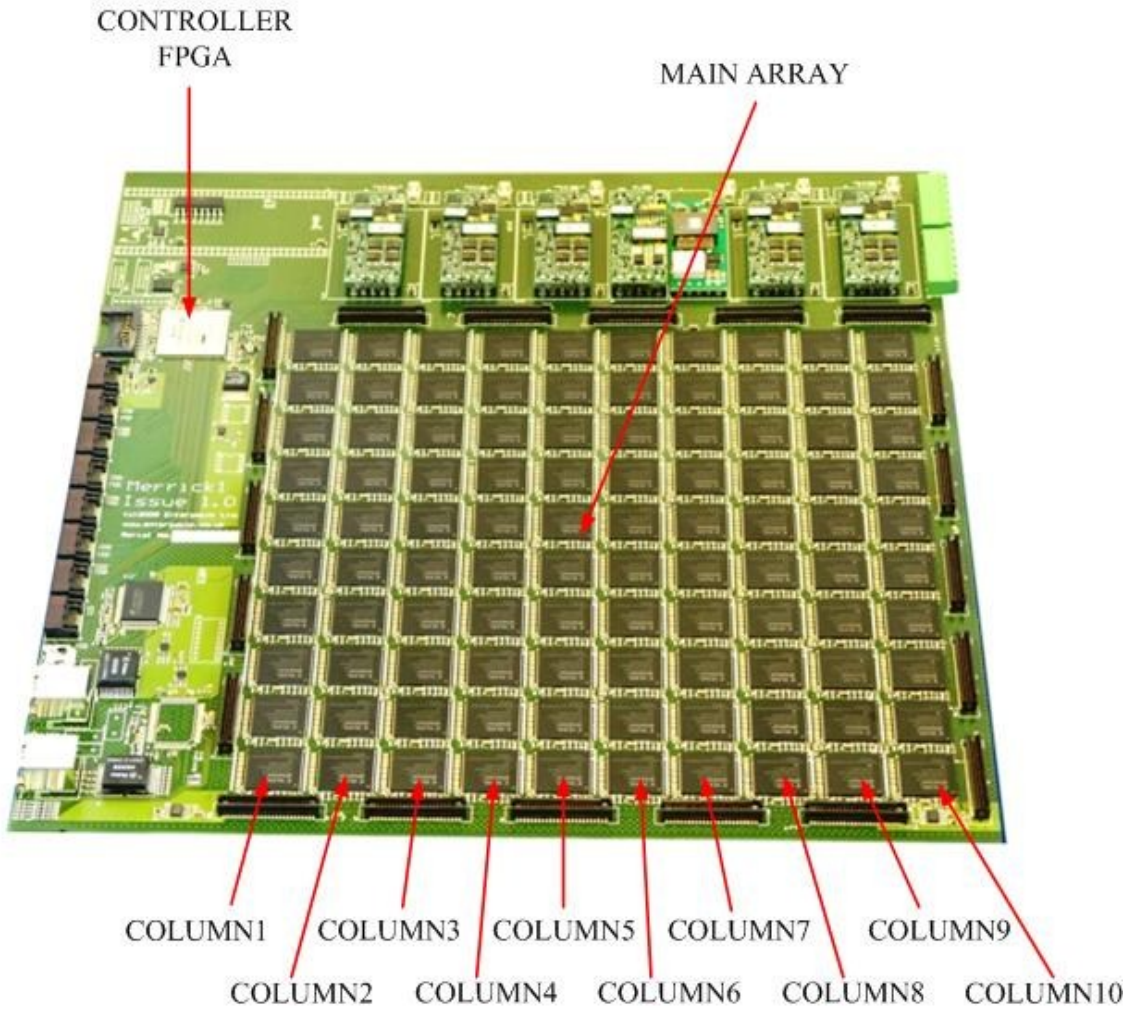


Figure7 – Merrick1 FPGAs

Main FPGA Array

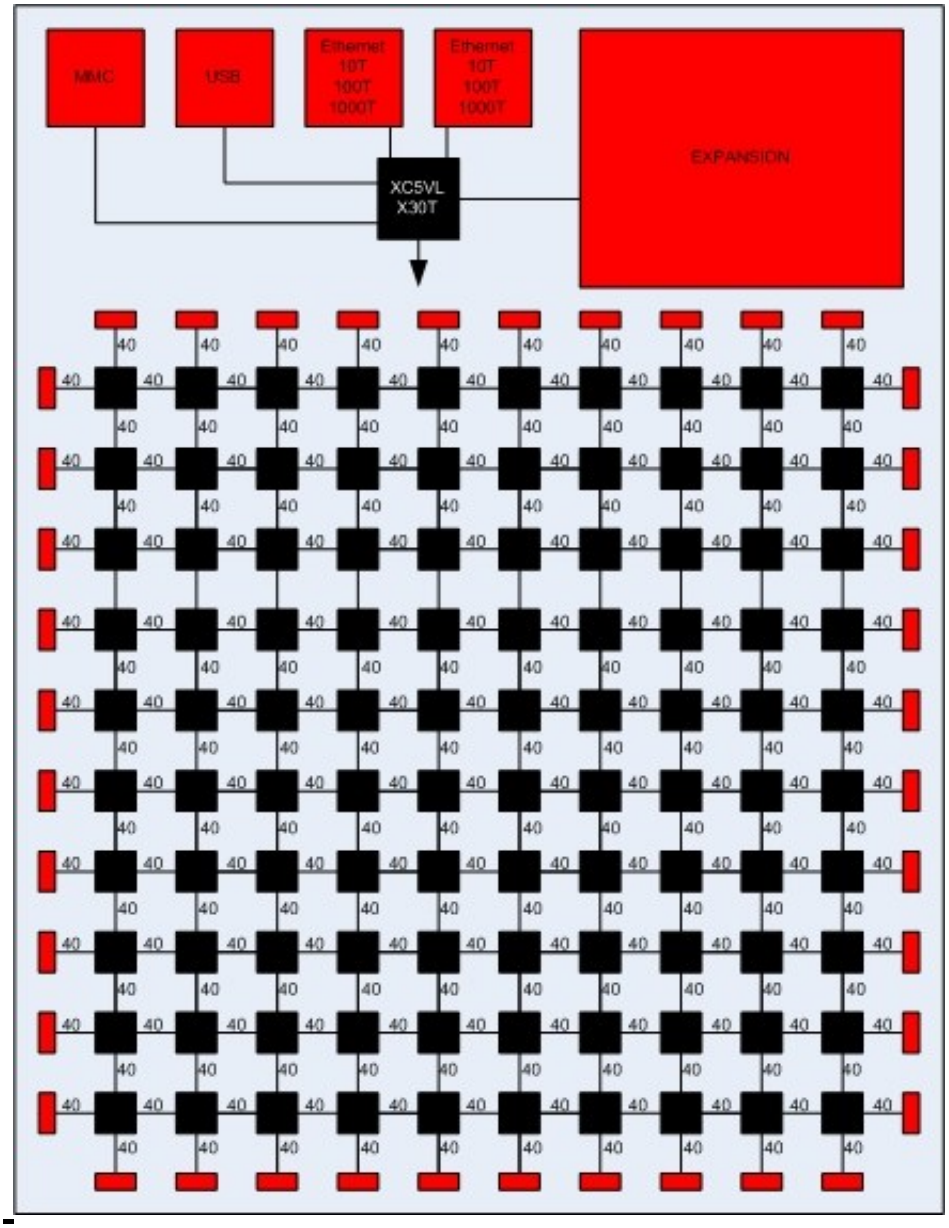


Figure8 – Interconnections on main array

The main feature of Merrick1 is a 10 x 10 array of Xilinx™ Spartan™-3A DSP XC3SD3400A-4CSG484C FPGAs. Each array FPGA has 40 wired connections on each side to its 4 adjacent FPGAs or I/O connectors. These are wired as differential pairs but may be used single ended. The I/O voltage is fixed at 2.5V. Using a standard configuration of 20 wires in each direction, LVDS as I/O standard, it is possible to implement a connection scheme of 1 forward clock + 1 alignment strobe + 8 data lines giving 500+ Mbyte/s between adjacent FPGAs in each direction.
1600 user I/O are available around the edges of the main FPGA array on the 40 50-way connectors. 20 are on the upper surface of the board and 20 on the underside. The connectors used are Vertical boxed 2x25 1.27mm IDC connectors (compatible with TDI type 222804-00225). 3.3V and 0V are also available on these connectors. Each connector is dedicated to a single FPGA and supports 20 pairs of LVDS or 40 single ended signals for High speed signalling.

Each individual FPGA has 174 connections in total. There are 40 signals on each side of each FPGA which connect to the neighbouring FPGAs so that the LEFT1 connection of one FPGA connects to the RIGHT1 connection of its left hand side neighbour. Similarly the TOP1 connection of one FPGA connects to the BOTTOM1 connection of the FPGA immediately above it in the array. There are also 14 connections which are daisy-chained along each column of 10 FPGAs and connect to the Controller FPGA, which are referred to as CLOCK signals The pinout of each Array FPGA is shown below:

SIGNAL NUMBER	RIGHT	LEFT	BOTTOM	TOP	CLOCK
0					AA14
1	G3	F19	B3	Y4	AB13
2	F3	F18	A3	W5	V12
3	C1	D21	D5	AA4	U12
4	C2	D22	C4	AB4	R18
5	F5	F21	B4	AB6	P19
6	F4	E20	A4	AB5	B9
7	H4	H22	F8	V8	A9
8	H3	G22	E8	W8	D6
9	H1	J19	C7	AA8	C6
10	G1	H20	D7	AB7	F16
11	R5	N21	B6	U9	E16
12	P4	M20	A7	V10	K3
13	E4	D20	A6	U8	K2
14	E3	E19	A5	V7	
15	N1	N22	G8	AA10	
16	M1	M22	F9	AB10	
17	P2	N20	D9	Y9	
18	P1	N19	C8	Y8	
19	R1	R22	B11	U10	
20	R2	P22	A11	V11	
21	J1	K20	C9	Y10	
22	H2	J20	D10	T11	
23	U5	U22	E13	AB14	
24	U4	T22	D13	AA15	
25	L1	L22	C13	W14	
26	K1	K22	C12	Y13	
27	U1	U20	B20	AB20	
28	T1	T20	A19	AA20	
29	T4	R19	B15	U15	
30	R3	R20	A14	U14	
31	W2	W22	A17	Y19	
32	W3	Y22	A16	Y18	
33	M2	K19	D19	AA19	
34	L3	K18	C19	AB19	
35	V3	W19	C15	V16	
36	V4	V20	D14	U16	
37	W1	Y21	C17	Y16	
38	Y1	AA22	B17	Y17	
39	V1	U18	C18	AB17	
40	U2	U19	B19	AB18	

The FPGAs at the edges of the array connect to 50-way 1.27mm IDC connectors along one side instead of interfacing to the neighbouring FPGA. The connections between the FPGAs and connectors are shown below:

CONNECTOR PIN	FPGA PIN			
	TOP CONNECTOR	BOTTOM CONNECTOR	LEFT CONNECTOR	RIGHT CONNECTOR
1	GND	GND	GND	GND
2	GND	GND	GND	GND
3	Y4	B3	F19	C1
4	W5	A3	F18	C2
5	AA4	D5	D21	E4
6	AB4	C4	D22	E3
7	AB6	B4	F21	F5
8	AB5	A4	E20	F4
9	U8	A6	D20	G3
10	V7	A5	E19	F3
11	U9	B6	J19	H1
12	V10	A7	H20	G1
13	3.3V	3.3V	3.3V	3.3V
14	3.3V	3.3V	3.3V	3.3V
15	V8	F8	H22	H4
16	W8	E8	G22	H3
17	AA8	C7	K20	J1
18	AB7	D7	J20	H2
19	AA10	G8	L22	L1
20	AB10	F9	K22	K1
21	Y9	D9	K19	M2
22	Y8	C8	K18	L3
23	Y10	C9	N21	N1
24	T11	D10	M20	M1
25	GND	GND	GND	GND
26	GND	GND	GND	GND
27	U10	B11	N22	R5
28	V11	A11	M22	P4
29	W14	C13	N20	P2
30	Y13	C12	N19	P1
31	AB14	E13	R22	R1
32	AA15	D13	P22	R2
33	U15	B15	R19	T4
34	U14	A14	R20	R3
35	V16	C15	U22	U1
36	U16	D14	T22	T1
37	3.3V	3.3V	3.3V	3.3V
38	3.3V	3.3V	3.3V	3.3V
39	Y16	C17	U20	U5
40	Y17	B17	T20	U4
41	Y19	A17	U18	V1
42	Y18	A16	U19	U2
43	AB17	C18	W19	V3
44	AB18	B19	V20	V4
45	AA19	D19	W22	W1
46	AB19	C19	Y22	Y1
47	AB20	B20	Y21	W2
48	AA20	A19	AA22	W3
49	GND	GND	GND	GND
50	GND	GND	GND	GND

The connector pins are defined as follows, viewed from above:

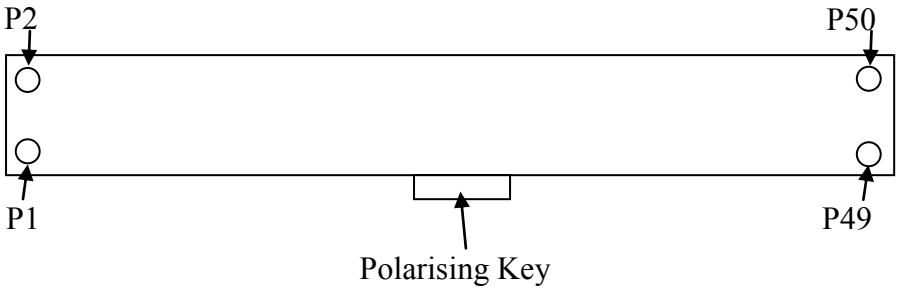


Figure9 – Merrick1 Connector pinout

Merrick Peripherals

MMC Interface

There is an SD Secure Digital Card Connector (compatible with Toby type 412D02F-09PC003) on Merrick which connects to the Controller FPGA. The connections between the Controller and the card connector are shown below:

CARD READER CONNECTION	SIGNAL NAME	FPGA PIN
WP1	MMC_WP1	B22
WP2	MMC_WP2	D21
CD1	MMC_CD1	A22
CD2	MMC_CD2	A23
1	MMC_CD/DAT_3	B21
2	MMC_CMD	C19
5	MMC_CLK	C21
7	MMC_DAT0	A24
8	MMC_DAT1	D19
9	MMC_DAT2	B20
POWER CONTROL	MMC_VD3V3_ON_N	C22

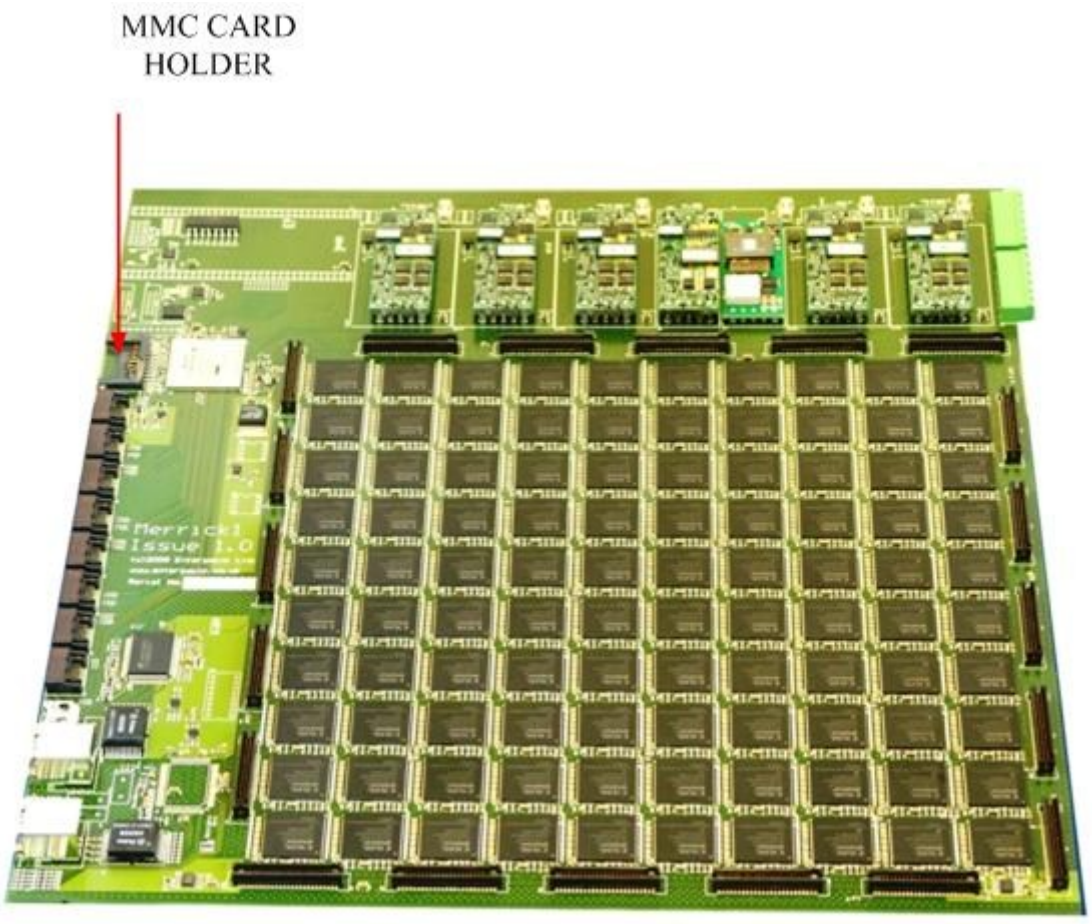


Figure10 - Merrick1 MMC Card Holder

Clock Generator 1

Merrick1 has a Cypress CY22394 three-PLL Serial-Programmable Clock Generator which provides clock signals to the Controller FPGA. It has a crystal oscillator source. Further information concerning this device can be found at www.cypress.com The connections between the Controller FPGA and the CY22394 device are shown below. All these connections are to Global Clock inputs on the Controller FPGA.

CY22394 PIN	SIGNAL NAME	FPGA PIN
10	CLK_A	AB15
9	CLK_B	AC16
1	CLK_C	AB16
6	CLK_X	AC17
16	CLK_SHUTDOWN_N	AC12
15	CLK_SUSPEND_N	AC13
7	CLK-P	AB17
8	CLK+P	AC18
13	CLK_SCLK	AC14
12	CLK_SDAT	AB14

Clock Generator 2

Merrick1's second clock generator is an ICS844071 Crystal-To-LVDS Clock Generator which has one differential LVDS output for high speed serial interfaces. It is intended to be used as the SATA clock, in which case a 25MHz oscillator should be used in the 8 pin 3.3V DIL socket J72. The ICS844071 has excellent <1ps phase jitter performance. For further information on this device please refer to www.idt.com. The output of this Clock generator is connected into the four MGTREFCLK inputs of the Controller FPGA i.e. K4,K3,T4,T3,D4,D3 and AB4,AB3.

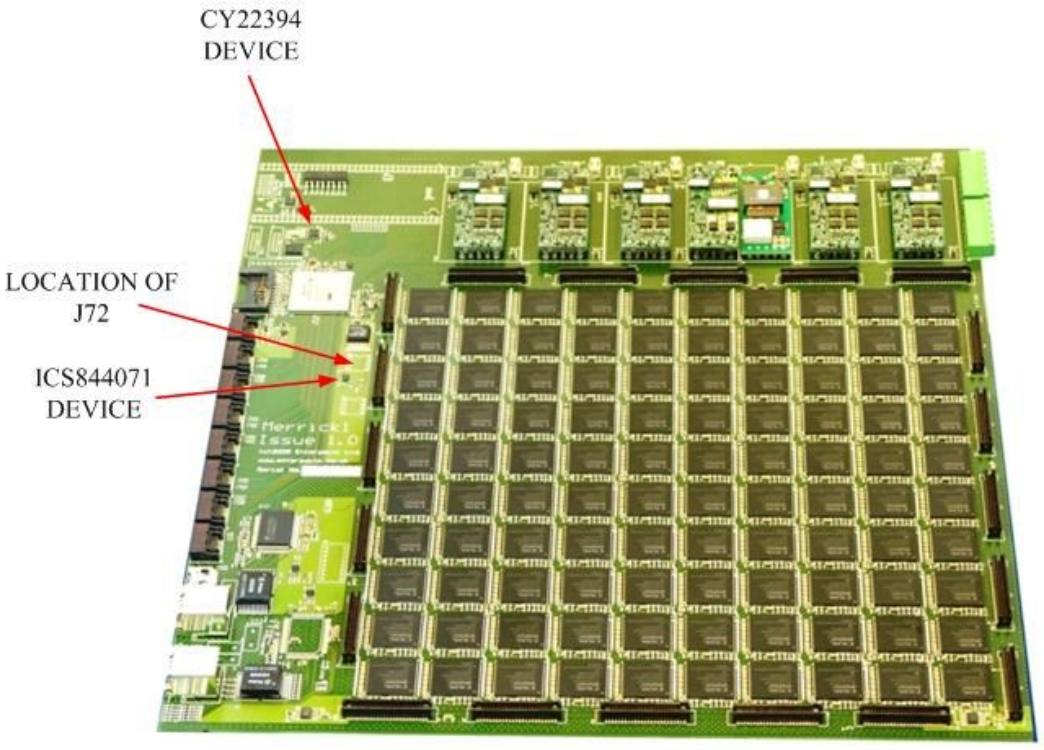


Figure11 – Merrick1 Clock Generators

Thermal Management and Fan Connectors

Merrick1 can run simple tasks with passive cooling but will require active cooling by fans and heatsinks to maximise performance. We have a range of cooling support options for this board. Please contact us for more information.
Merrick1 has four 3 pin fan connectors with rpm monitoring capability. The pinout of the fan connectors is:

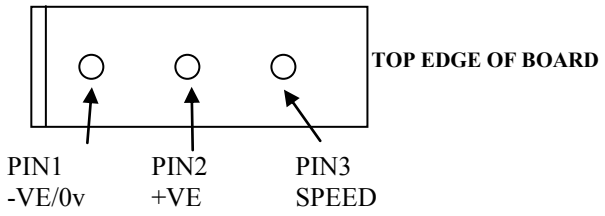


Figure 12 - Merrick1 fan connector pinout

By default the fan connectors connect between the main 48V supply, but a header (J73) is provided so that the user can connect an alternative fan power supply, which must be reference to the main input 0V. The user's fan supply should be connected with +ve on pin 3 and 0V on pin2 of J73. **If 48V fans are fitted it is necessary to link from J73 Pin 1 to Pin3 otherwise the fans will not be powered.**

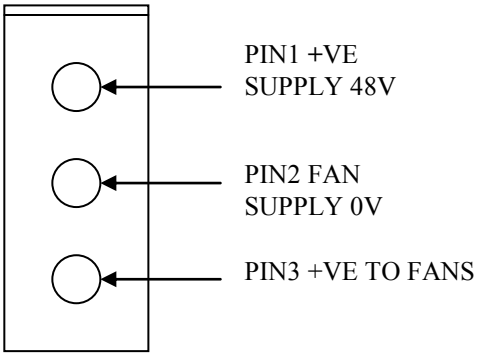


Figure 13 - J73 connections

The four 'fan speed' signals are routed to the Controller FPGA via optocouplers to protect the FPGA input circuitry. The connections to the Controller FPGA are shown below:

FAN	CONNECTOR	FPGA PIN
1	J3	A20
2	J4	A25
3	J5	D20
4	J6	A18

The optocouplers each have a jumper (J7, J8, J9 and J50) which should be fitted if the fan speed signal is being used.

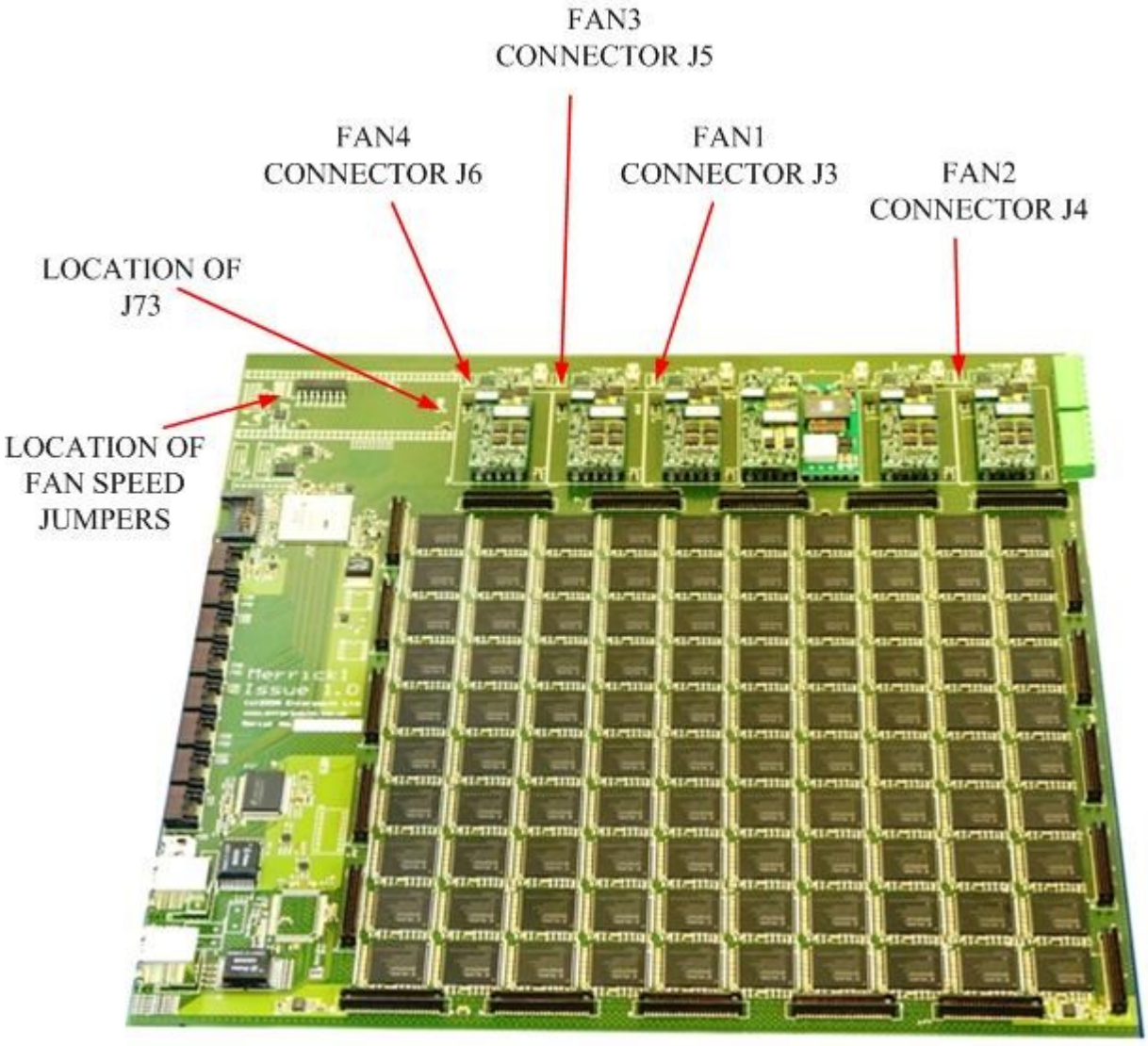


Figure 14 – Merrick1 Fan Connectors

DIL Headers

The DIL Headers provide a simple mechanical and electrical interface for add-on modules. The connectors on this header are on a 0.1inch, 2.54mm, pitch and allow either custom modules or strip board to be fitted. The headers have a row of permanent positive power sockets (3.3V) above J58 and a row of permanent GND (0V) sockets below J57.

There are 20 IOs routed from the Controller FPGA to the DIL headers. The remaining pins are used for mechanical support and for power supply (3.3V and 0V) to the modules or user add-on board. Voltages outside the range 0V to 3.3V must not be applied to the DIL headers. The Virtex5 has an absolute maximum IO input voltage of 4V.

The connections between the DIL the headers and the Controller FPGA are shown below:

LEFT EDGE OF BOARD				
J58			J57	
C11	3.3V		0V	B4
D11	3.3V		0V	B5
B12	3.3V		0V	D5
C12	3.3V		0V	E5
R8	3.3V		0V	M6
R7	3.3V		0V	N7
N8	3.3V		0V	P6
P8	3.3V		0V	N6
T7	3.3V		0V	A12
E22	3.3V		0V	H19
	3.3V		0V	
	3.3V		0V	
	3.3V		0V	
	3.3V		0V	
	3.3V		0V	
	3.3V		0V	
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	3.3V		0V	

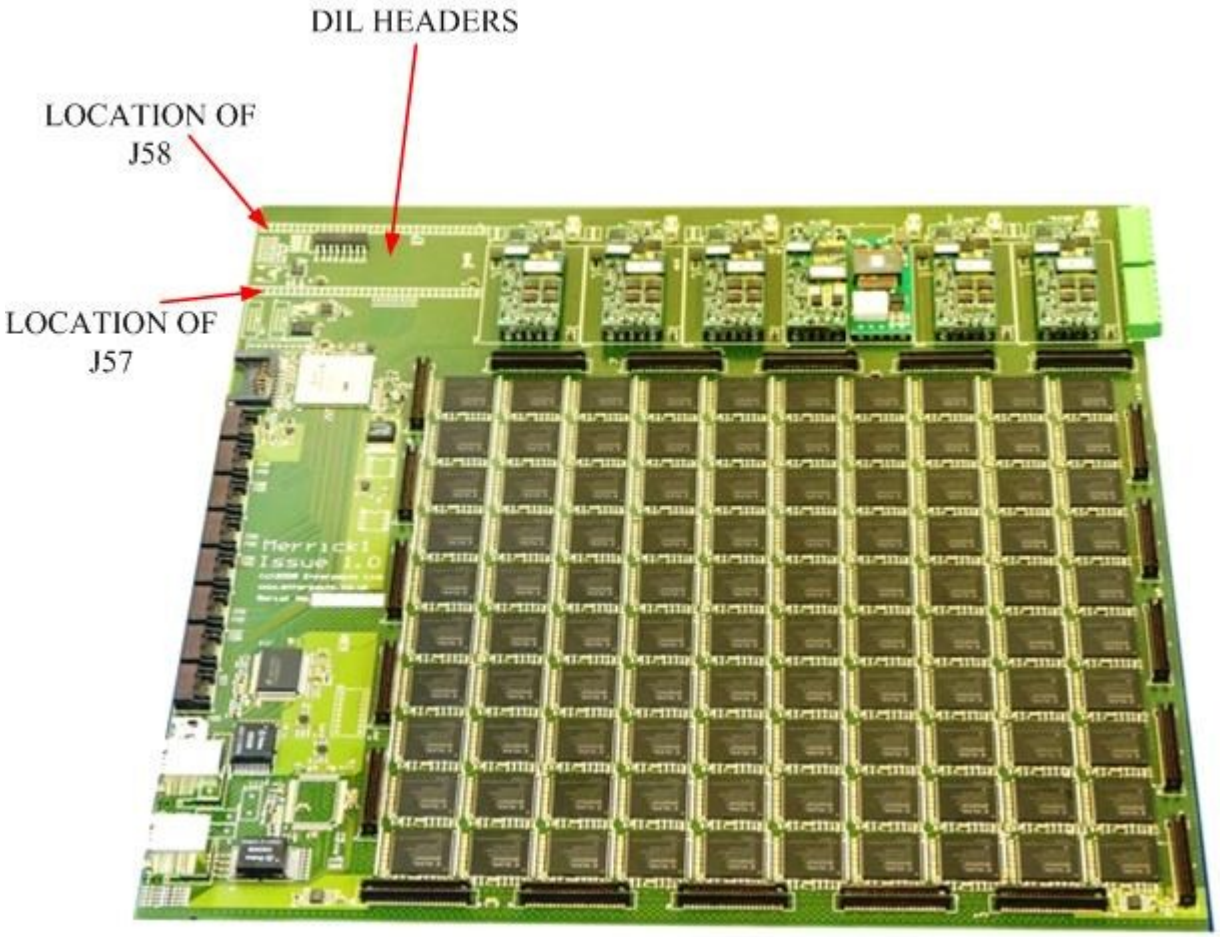


Figure 15 – Merrick1 DIL Headers

Oscillator

There are 2 oscillator sockets on Merrick1 for users to select their own oscillator frequency. These support 3.3V, 8-pin DIL outline, oscillator crystals. One of these is dedicated to the SATA clock generator. There is also a fixed 25MHz oscillator and a 0-400MHz clock generator which has a crystal oscillator source.

The fixed 25MHz signal is routed directly to the Controller FPGA pin **AC19**, which is a Global Clock input.

The Virtex5 LX30T has two Clock Management tiles, each of which contains two Digital Clock Multipliers and one Phase Locked Loop. to produce multiples, divisions and phases of clock signals. Please consult the Virtex5 datasheet available from the Xilinx website at http://www.xilinx.com if multiple clock signals are required.

User LEDs

On Merrick1 there are 8 LEDS which connect to the Controller FPGA and one on each of the 100 Array FPGAs. These are all user-controllable LEDs and are connected to the FPGAs as indicated below:

HOST DEVICE	DESIGNATOR	FPGA PIN
Controller FPGA	LED2	C13
	LED3	C14
	LED4	B14
	LED5	A13
	LED6	A14
	LED7	A15
	LED8	B15
	LED9	C16
Array FPGAs	LED1	E7

Additionally there are 5 LEDs connected to each Ethernet Controller device. These are not available for user control. There are also 7 LEDs indicating the presence of power from 7 of the 8 power modules.

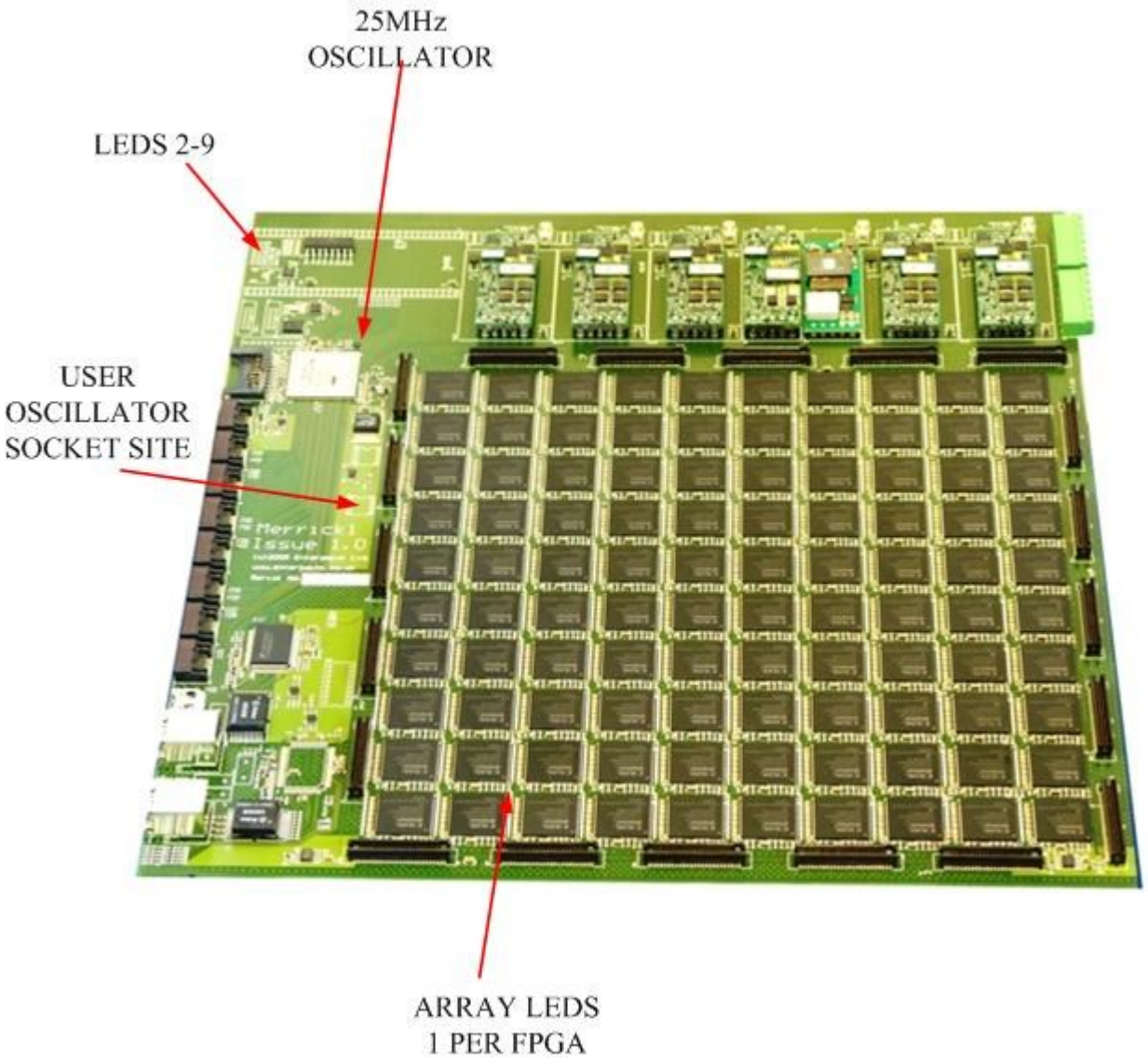


Figure 16 – Merrick1 Oscillators and LEDs

USB

The USB interface on the Merrick1 is achieved using an FT232R USB to serial UART interface and a Mini-B type connector. The datasheet and drivers for this device are available from http://www.ftdichip.com. When appropriate drivers are installed the Merrick1 USB port should be detected as a serial port. Alternative data optimised drivers are also available from FTDI.

The FT232R is connected to the Controller FPGA and provided a simple UART, or other converter, is implemented then the data sent over the USB serial port can be used either as control and/or data information. This allows a host computer to act in a number of ways including system control and data storage functions. The connections between the USB device and the FPGA are shown below:

FT232R	FPGA PIN
CTS#	C24
DCD#	B26
DSR#	D23
RI#	D24
RTS#	C23
DTR#	B25
TXD	B24
RXD	C26

Switches

Merrick1 has a bank of 8 2-position DIP switches. To use these switches it is necessary to set the IO pins connected to the switches to have a pull up resistor setting in the constraints file. The switches are connected to the following IO pins. Switch 1 is furthest from the Virtex5 device.

SWITCH	FPGA PIN
1	AA5
2	AB5
3	AB6
4	AB7
5	AE6
6	AF5
7	AE5
8	AD4

Battery Backup

The Merrick1 has a battery holder which is available to provide battery backup to the FPGA. It is connected to the Controller FPGA on Pin J19. The battery holder accepts a 3V Lithium battery size CR1220 or equivalent. Battery backup allows the use of an encrypted bitstream for the Controller FPGA and facilitates IP locking to an individual board etc.

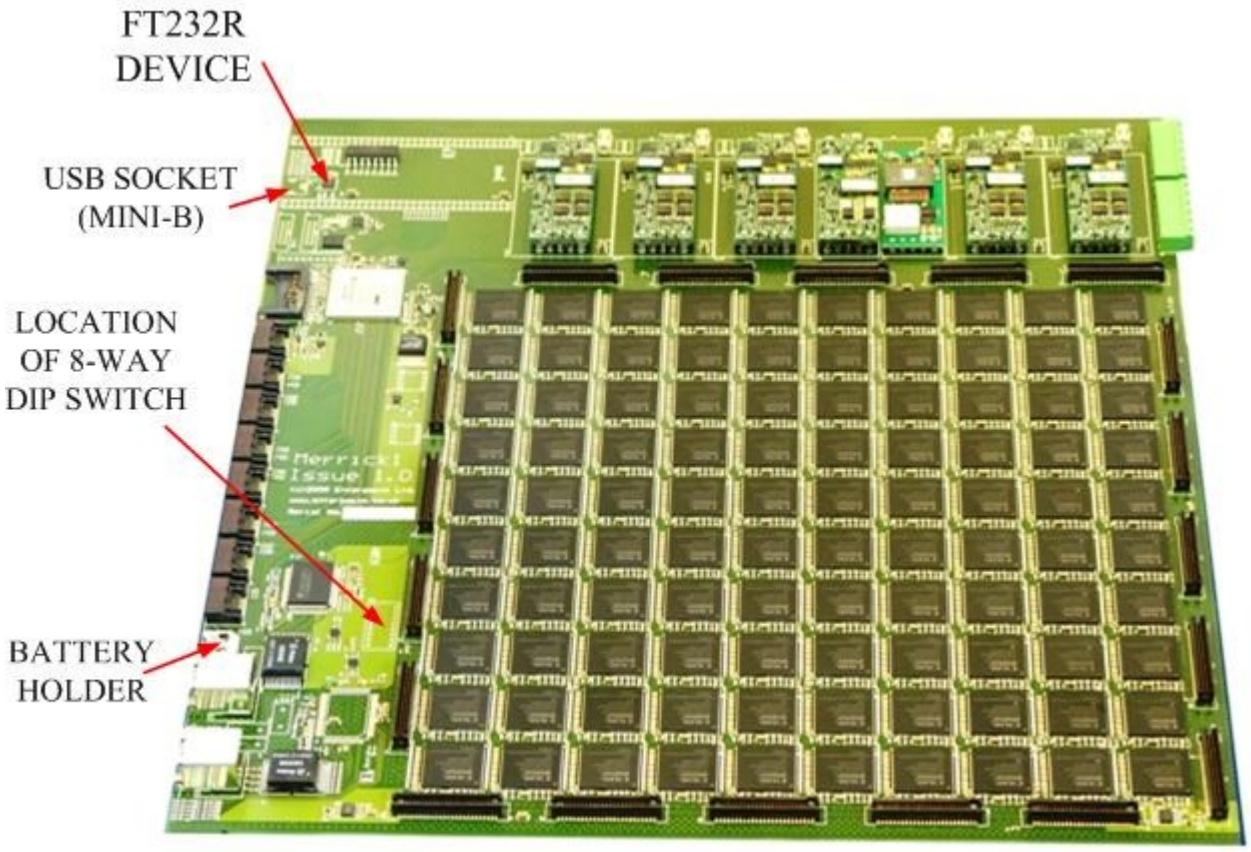


Figure 17 – Merrick1 USB, Switches and Battery

SATA

Merrick1 has 8 SATA connectors which are connected to the MGT interface of the Controller FPGA. An ICS844071 is used to generate the SATA Clock. The connections between the SATA Clock, the SATA connectors and the FPGA are shown below (omitting series capacitors, J56 being nearest to the Controller FPGA and J69 the furthest). Each pair of SATA Clock connections supplies 2 sets of SATA inputs. Half the 8 channels have their TX and RX connections reversed to allow board stacking connections using standard SATA cables.

J56 PIN	FPGA PIN	J67 PIN	FPGA PIN	J62 PIN	FPGA PIN	J63 PIN	FPGA PIN
PIN 2	B2	PIN 2	G2	PIN 2	H2	PIN 2	N2
PIN 3	C2	PIN 3	F2	PIN 3	J2	PIN 3	M2
PIN 5	C1	PIN 5	F1	PIN 5	J1	PIN 5	M1
PIN 6	D1	PIN 6	E1	PIN 6	K1	PIN 6	L1
CLOCK+	D4	CLOCK+	D4	CLOCK+	K4	CLOCK+	K4
CLOCK-	D3	CLOCK-	D3	CLOCK-	K3	CLOCK-	K3

J64 PIN	FPGA PIN	J65 PIN	FPGA PIN	J68 PIN	FPGA PIN	J69 PIN	FPGA PIN
PIN 2	P2	PIN 2	W2	PIN 2	Y2	PIN 2	AD2
PIN 3	R2	PIN 3	V2	PIN 3	AA2	PIN 3	AE2
PIN 5	R1	PIN 5	V1	PIN 5	AA1	PIN 5	AD1
PIN 6	T1	PIN 6	U1	PIN 6	AB1	PIN 6	AC1
CLOCK+	T4	CLOCK+	T4	CLOCK+	AB4	CLOCK+	AB4
CLOCK-	T3	CLOCK-	T3	CLOCK-	AB3	CLOCK-	AB3

Figure 18 – Merrick1 SATA Connectors

Ethernet Interface

Merrick1 has two 10/100/1000 base-T connections which interface to the MAC hard IP cores within the Controller FPGA. The Ethernet signals each pass through a transformer to a DP8365DVH Ethernet Phy device. The signals are then passed to the Controller FPGA as shown below:

SIGNAL	ETHERNET1	ETHERNET2
ETH_RX0	A9	W5
ETH_RX1	A8	W6
ETH_RX2	E8	G4
ETH_RX3	E7	H4
ETH_RX4	B9	V6
ETH_RX5	C8	V7
ETH_RX6	E6	J5
ETH_RX7	D6	J6
ETH_TX0	H7	Y6
ETH_TX1	G7	Y5
ETH_TX2	F7	G6
ETH_TX3	F8	H6
ETH_TX4	F9	Y4
ETH_TX5	G9	W4
ETH_TX6	H8	G5
ETH_TX7	J8	F5
ETH_CK_MAC_FREQ	B11	R6
ETH_TX_ER	C9	U7
ETH_TXEN_ER	D8	T8
ETH_SEL1	C7	K5
ETH_SEL0	C6	L5
ETH_TCK	A7	K6
ETH_MDIO	B7	K7
ETH_MDC	D10	U6
CLOCK_ETH_25MHZ	B6	U5
ETH_RESET_N	B6	K8
ETH_CLK_TO_MAC	A5	L7
ETH2_INT_N	B10	T5
ETH2_RXDV_ER	A10	R5
ETH2_RCK	A4	M7
ETH2_RX_CLK	A3	L8

SPI Flash Memory

The M25P128 SPI flash memory device configures the Controller FPGA when it is powered providing a suitable bitstream is programmed into the device. The M25P128 has a capacity of 128Mbits with a single configuration bitstream for Merrick1 Controller FPGA taking 3.2MB. Any remaining space can be used for alternative configurations or code and data storage e.g. Microblaze™ code.

The HOLD pin of this memory device is permanently connected to 3.3V. After configuration the SPI Flash can be accessed via the following pins of the FPGA:

M25P128 FUNCTION	FPGA PIN
CCLK	J11
MOSI	AA12
WRITE_SPI	D26
DIN	J10
CSO_B	Y12

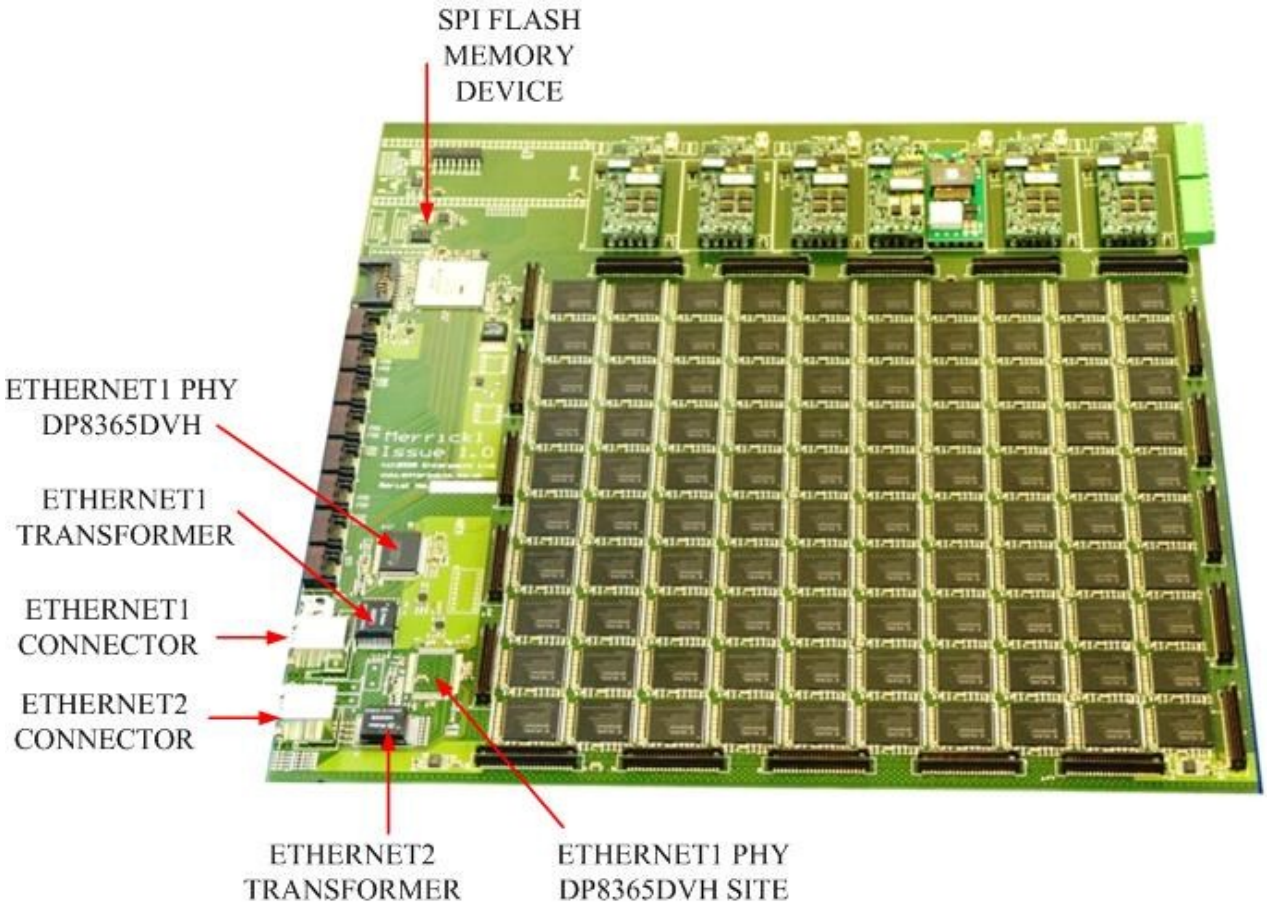


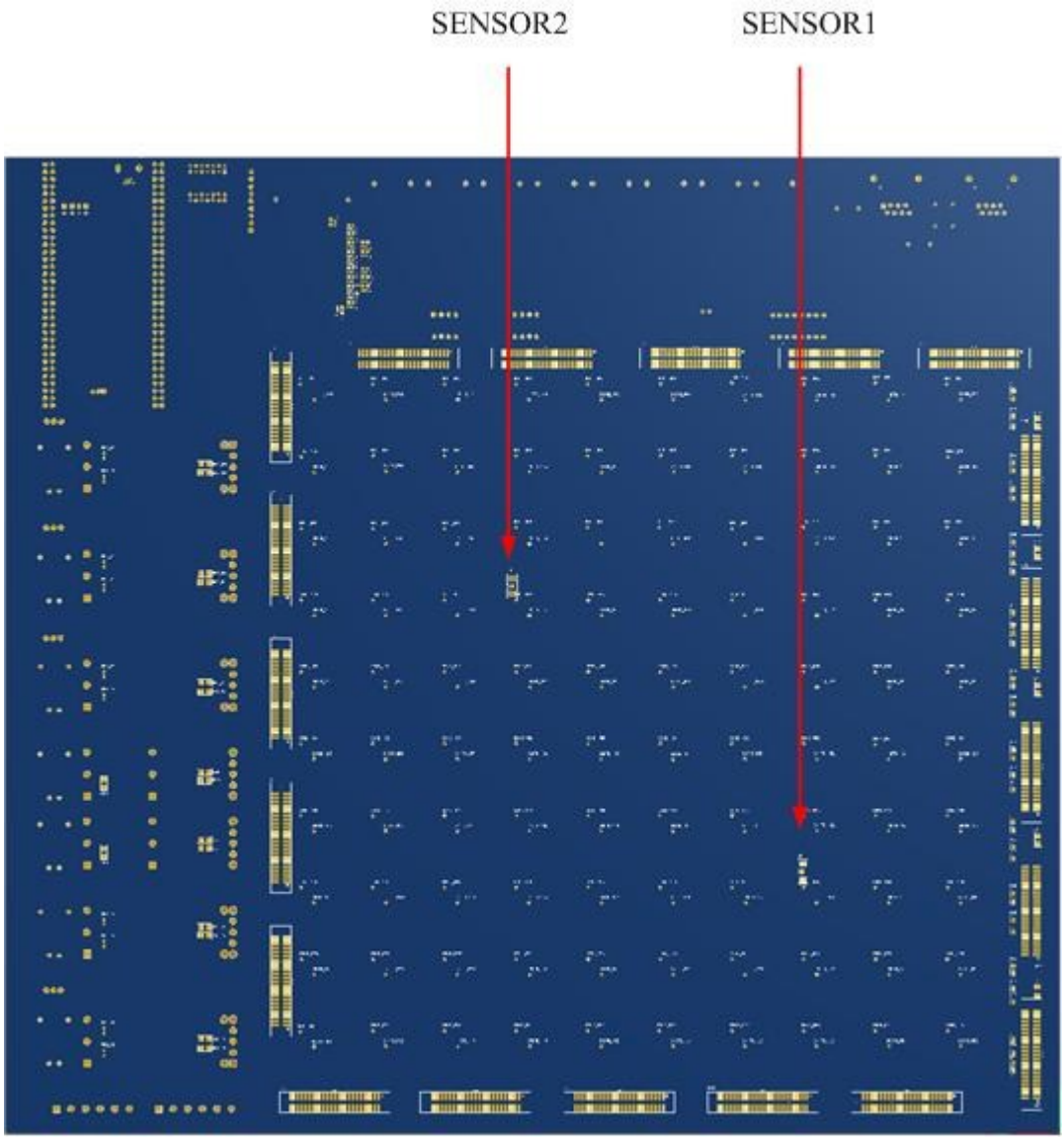
Figure 19 – Merrick1 Ethernet and SPI Flash Memory

Temperature Sensors

There are two temperature sensors (type LM75C) on Merrick1 which have a 2-wire serial interface and outputs which behave as over-temperature warnings. The connections to the Controller FPGA are shown below:

SIGNAL	FPGA PIN (SENSOR1)	FPGA PIN (SENSOR2)
SDA	W11	AA19
SCL	Y10	Y11
OVER-TEMPERATURE	Y20	AA18

The temperature sensors are located on the underside of the board:



Mechanical Information

The Merrick1 board is designed to fit into a standard 9U rack.

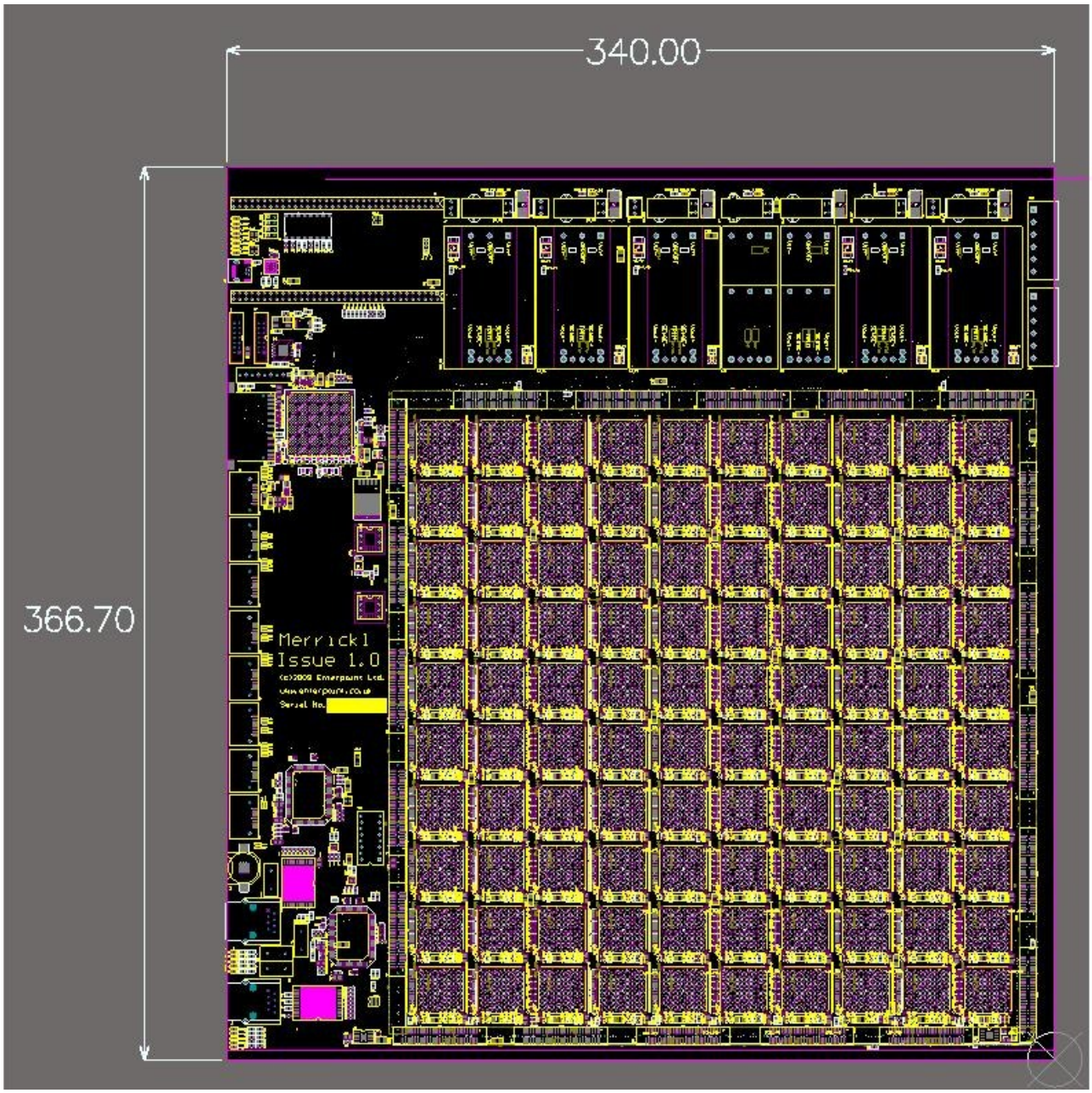


Figure 20 – Mechanical Arrangement of Merrick1

All dimensions are shown in millimetres. If you need any further mechanical information please contact us. Contact information is shown on page 34 of this manual.

Medical and Safety Critical Use

Merrick1 boards are not authorised for the use in, or use in the design of, medical or other safety critical systems without the express written person of the Board of Enterpoint. If such use is allowed the said use will be entirely the responsibility of the user. Enterpoint Ltd will accepts no liability for any failure or defect of the Merrick1 board, or its design, when it is used in any medical or safety critical application.

Warranty

Merrick1 comes with a 90 day return to base warranty. Do not attempt to solder connections to the Merrick1. Enterpoint reserves the right not honour a warranty if the failure is due to soldering or other maltreatment of the Merrick1 board.

Outside warranty Enterpoint offers a fixed price repair or replacement service. We reserve the right not to offer this service where a Merrick1 has been maltreated or otherwise deliberately damaged. Please contact support if need to use this service.

Other specialised warranty programs can be offered to users of multiple Enterpoint products. Please contact sales on boardsales@enterpoint.co.uk if you are interested in these types of warranty,

Support

Enterpoint offers support during normal United Kingdom working hours 9.00am to 5.00pm. Please examine our Merrick1 FAQ web page and the contents of this manual before raising a support query. We can be contacted as follows:

Telephone - ++44 (0) 121 288 3945
Email - support@enterpoint.co.uk

Backup Support

We can offer a guaranteed product replacement plan to purchasers of Merrick1. For a fixed monthly fee you get a time guaranteed replacement board if your board should fail in service. Please contact us for more details of this service